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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,057	04/21/2004	Charles Norman Shaver	200314194-1	5954

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EXAMINER	
SPITTLE, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,057	SHAVER ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-11 and 13-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-11 and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1, 2, 4 – 11, and 13 – 18 have been examined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 4, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belkin Components (Hi-Speed USB 2.0 4-Port Drive Bay Hub User Manual), hereafter referred to as Belkin, in view of Cables To Go, hereafter referred to as CTG, Alcor, and Belkin Components (USB 2.0 Hi-Speed PCI Card User Manual), hereafter referred to as Belkin2, and evidence as provided by the USB 2.0 Specification.

Regarding claim 1, Belkin teaches a system for providing a USB port within a computer chassis comprising:

A printed wire board (PWB) (shown in the Figure on page 1) supporting a second USB header (interpreted as a USB connector; Page 5, #4), a third USB header (interpreted as the inherent connective PCB traces that connects any of the external USB ports as shown in the Figure on page 1), the PWB being mountable at a location within the computer chassis (Page 4, Figure 2 shows the device being installed within the computer chassis);

The third USB header (interpreted as the inherent connective PCB traces that connects any of the external USB ports as shown in the Figure on page 1) operative to communicate with the external USB port (4 external USB ports are shown on page 1, Figure 1);

Belkin fails to explicitly teach a USB hub, a motherboard having a first USB header, the second USB header operative to communicate with the first USB header, a voltage regulator, and an internal USB port.

Alcor teaches a USB hub controller for providing a plurality of USB ports to connect USB devices in a cost-effective manner that provides power switch control and over-current sensing (Page 1).

Alcor also teaches a voltage regulator, the voltage regulator being operative to receive a first voltage output from the motherboard (Where the voltage regulator receives this power on pin 10 of the hub controller chip (pages 5 – 6), and to provide in response thereto, a second, lower voltage output to the USB hub (Page 1, Section 1.2).

CTG teaches a motherboard having a first USB header (Product Features, paragraph 1; Installation Guide, Step 5-1), as well as a second header (interpreted as

the connective wiring that connects the motherboard header to the external USB port as shown in the Figure on the Product Features page).

Belkin2 teaches an internal USB port (Page 5, PORT 5) for the purpose of providing USB functionality to internal USB devices.

It would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate an internal USB port as taught by Belkin2 into the USB hub device of Belkin for the purpose of adding the capability to connect internal USB devices. This would have been obvious because some internal devices (such as card readers, hard drives, etc) require an internal USB connection.

It would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to utilize the USB hub controller as taught by Alcor in controlling the USB ports of Belkin, and Belkin2 in a cost-effective manner that provides power switch control and over-current sensing. This would have been obvious in order to avoid damaging the attached USB devices.

Examiner notes that the hub controller of Alcor requires an upstream connection to a USB host controller as shown on page 3. One of ordinary skill in this art would find it obvious to make this connection by attaching the pins of the controller (via a second USB header as claimed) through the cable of CTG to the motherboard USB header of CTG. This would have been obvious since a USB system requires a host controller to operate, and the cable of CTG would be one method of making this connection.

Regarding claim 2, Belkin teaches the additional limitation wherein the location at which the PWB is mounted is a location other than a Peripheral Component Interface (PCI) expansion slot of the computer chassis (Belkin shows the PWB mounted in a 3.5" drive bay; page 4, Figure 2).

Regarding claim 4, Alcor teaches the additional limitation wherein the first voltage output is approximately 5 volts, and the second voltage output is approximately 3.3 volts (Page 1, Section 1.2; Page 6, pins 10, 12).

Regarding claim 5, CTG teaches the additional limitation wherein the PWB is operative to receive a third voltage output from the motherboard, the third voltage output being routed by the PWB to power the external USB port (Examiner notes that the USB bus inherently carries a voltage output on its Vbus line, as evidenced by the USB 2.0 Specification, page 18, lines 1 – 2. Thus, if the motherboard is "providing" the USB bus to the PWB via the CTG cable, then the motherboard is implicitly providing a voltage output (Vbus)).

Regarding claim 8, CTG teaches the additional limitation of the system further comprising:

A first USB cable operative to interconnect the first USB header of the motherboard with the second USB header (Product Features, see "Motherboard cable");

A second USB cable operative to interconnect the third USB header with the external USB port (Examiner notes that Belkin has attached the external USB port via the PCB traces to the third USB header. However, Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of invention by Applicant to replace the PCB traces with a cable for the purpose of flexibly positioning the USB port at a location other than attached directly to the USB hub device.).

* * *

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belkin Components (Hi-Speed USB 2.0 4-Port Drive Bay Hub User Manual), hereafter referred to as Belkin, in view of Cables To Go, hereafter referred to as CTG, Alcor, and Belkin Components (USB 2.0 Hi-Speed PCI Card User Manual), hereafter referred to as Belkin2, Le et al. (U.S. Pub. 2003/0210532) and evidence as provided by the USB 2.0 Specification.

Regarding claim 6, Belkin teaches a system for providing a USB port within a computer chassis comprising:

A printed wire board (PWB) (shown in the Figure on page 1) supporting a second USB header (interpreted as a USB connector; Page 5, #4), a third USB header (interpreted as the inherent connective PCB traces that connects any of the external USB ports as shown in the Figure on page 1), the PWB being mountable at a location

within the computer chassis (Page 4, Figure 2 shows the device being installed within the computer chassis);

The third USB header (interpreted as the inherent connective PCB traces that connects any of the external USB ports as shown in the Figure on page 1) operative to communicate with the external USB port (4 external USB ports are shown on page 1, Figure 1);

Belkin fails to explicitly teach a USB hub, a motherboard having a first USB header, the second USB header operative to communicate with the first USB header, a voltage regulator, and an internal USB port.

Alcor teaches a USB hub controller for providing a plurality of USB ports to connect USB devices in a cost-effective manner that provides power switch control and over-current sensing (Page 1).

CTG teaches a motherboard having a first USB header (Product Features, paragraph 1; Installation Guide, Step 5-1), as well as a second header (interpreted as the connective wiring that connects the motherboard header to the external USB port as shown in the Figure on the Product Features page).

Belkin2 teaches an internal USB port (Page 5, PORT 5) for the purpose of providing USB functionality to internal USB devices.

It would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate an internal USB port as taught by Belkin2 into the USB hub device of Belkin for the purpose of adding the capability to connect internal

USB devices. This would have been obvious because some internal devices (such as card readers, hard drives, etc) require an internal USB connection.

It would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to utilize the USB hub controller as taught by Alcor in controlling the USB ports of Belkin, and Belkin2 in a cost-effective manner that provides power switch control and over-current sensing. This would have been obvious in order to avoid damaging the attached USB devices.

Examiner notes that the hub controller of Alcor requires an upstream connection to a USB host controller as shown on page 3. One of ordinary skill in this art would find it obvious to make this connection by attaching the pins of the controller (via a second USB header as claimed) through the cable of CTG to the motherboard USB header of CTG. This would have been obvious since a USB system requires a host controller to operate, and the cable of CTG would be one method of making this connection.

Belkin, Belkin2, CTG, and Alcor fail to teach the chassis having mounts extending into the interior thereof and the PWB having apertures formed therethrough, each of the apertures being operative to receive one of the mounts such that insertion of the mounts into the apertures secures the PWB to the chassis.

Le et al. teach the chassis (Figures 3A, 3B, item 100) having mounts extending into the interior thereof (Figures 3A, 3B; items 333, 334);

The PWB has apertures formed therethrough, each of the apertures being operative to receive one of the mounts such that insertion of the mounts into ths

apertures secures the PWB to the chassis (where the PWB is interpreted in Figures 3A and 3B as item 220, and the apertures are interpreted as mounting holes (item 221).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the mounting means as taught by Le et al. into the system of Lelong et al. for the purpose of mounting the PWB in a secure manner to the chassis to prevent damage from occurring due to the PWB physically impacting the other components.

Regarding claim 7, Le et al. teach the additional limitation wherein the mounts form interference fits with the apertures when the mounts are inserted within the apertures (Figure 3A and 3B clearly show an interference fit between the mounts (items 333, 334) and the apertures (item 221)).

* * *

Claims 9 – 11, 13 – 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belkin Components (Hi-Speed USB 2.0 4-Port Drive Bay Hub User Manual), hereafter referred to as Belkin, in view of Cables To Go, hereafter referred to as CTG, Alcor, and Belkin Components (USB 2.0 Hi-Speed PCI Card User Manual), hereafter referred to as Belkin2, and evidence as provided by the USB 2.0 Specification.

Regarding claim 9, Belkin teaches a system for providing a USB port within a computer chassis comprising:

A chassis defining an interior (Page 4, Figure 2 shows a PC chassis);

A first Universal Serial Bus (USB) port externally mounted to the chassis (Page 4, Figure 2 shows 4 USB ports externally mounted to the chassis via the USB hub device);

A daughter card mounted within the interior of the chassis (Page 4, Figure 2 shows the USB hub device being mounted within the interior of the chassis), and having a second USB header (interpreted as a USB connector; Page 5, #4), and a third USB header (interpreted as the inherent connective PCB traces that connects any of the external USB ports as shown in the Figure on page 1);

Belkin fails to explicitly teach a USB hub, a motherboard having a first USB header, the second USB header operative to communicate with the first USB header, a voltage regulator, and an internal USB port.

Alcor teaches a USB hub controller for providing a plurality of USB ports to connect USB devices in a cost-effective manner that provides power switch control and over-current sensing (Page 1).

Alcor also teaches a voltage regulator, the voltage regulator being operative to receive a first voltage output from the motherboard (Where the voltage regulator receives this power on pin 10 of the hub controller chip (pages 5 – 6), and to provide in response thereto, a second, lower voltage output to the USB hub (Page 1, Section 1.2).

CTG teaches a motherboard having a first USB header (Product Features, paragraph 1; Installation Guide, Step 5-1), as well as a second header (interpreted as

the connective wiring that connects the motherboard header to the external USB port as shown in the Figure on the Product Features page).

Belkin2 teaches an internal USB port (Page 5, PORT 5) for the purpose of providing USB functionality to internal USB devices.

It would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate an internal USB port as taught by Belkin2 into the USB hub device of Belkin for the purpose of adding the capability to connect internal USB devices. This would have been obvious because some internal devices (such as card readers, hard drives, etc) require an internal USB connection.

It would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to utilize the USB hub controller as taught by Alcor in controlling the USB ports of Belkin, and Belkin2 in a cost-effective manner that provides power switch control and over-current sensing. This would have been obvious in order to avoid damaging the attached USB devices.

Examiner notes that the hub controller of Alcor requires an upstream connection to a USB host controller as shown on page 3. One of ordinary skill in this art would find it obvious to make this connection by attaching the pins of the controller (via a second USB header as claimed) through the cable of CTG to the motherboard USB header of CTG. This would have been obvious since a USB system requires a host controller to operate, and the cable of CTG would be one method of making this connection.

Regarding claim 10, CTG teaches the additional limitation wherein the chassis has a Peripheral Component Interface (PCI) expansion slot (Installation Guide, see the slots shown in Step 5-2), and the daughter card is mounted at a location other than the PCI expansion slot (Installation Guide, Step 3 #2 shows the daughter card mounted in a drive bay).

Regarding claim 11, CTG teaches the additional limitation wherein the motherboard controls continuity of power to the daughter card (Examiner notes that the USB bus inherently carries a voltage output on its Vbus line, as evidenced by the USB 2.0 Specification, page 18, lines 1 – 2. Thus, if the motherboard is "providing" the USB bus to the PWB via the CTG cable, then the motherboard is implicitly providing a voltage output (Vbus). Voltage is related to power via Power = voltage * current, and therefore the motherboard is controlling the continuity of power to the daughter card.

Regarding claim 13, Alcor teaches the additional limitation wherein the first voltage output is approximately 5 volts, and the second voltage output is approximately 3.3 volts (Page 1, Section 1.2; Page 6, pins 10, 12).

Regarding claim 14, CTG teaches the additional limitation wherein the daughter card is operative to receive a third voltage output from the motherboard, the third voltage output being routed by the daughter card to power the external USB port (Examiner notes that the USB bus inherently carries a voltage output on its Vbus line,

as evidenced by the USB 2.0 Specification, page 18, lines 1 – 2. Thus, if the motherboard is "providing" the USB bus to the daughter card via the CTG cable, then the motherboard is implicitly providing a voltage output (Vbus)).

Regarding claim 15, CTG teaches the additional limitation wherein there is means for securing the daughter card to the chassis (Installation Guide, Step 3 #3).

Regarding claim 18, CTG teaches the additional limitation of the system further comprising:

A first USB cable operative to interconnect the first USB header of the motherboard with the second USB header (Product Features, see "Motherboard cable"); A second USB cable operative to interconnect the third USB header with the external USB port (Examiner notes that Belkin has attached the external USB port via the PCB traces to the third USB header. However, Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of invention by Applicant to replace the PCB traces with a cable for the purpose of flexibly positioning the USB port at a location other than attached directly to the USB hub device.).

* * *

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belkin Components (Hi-Speed USB 2.0 4-Port Drive Bay Hub User Manual),

hereafter referred to as Belkin, in view of Cables To Go, hereafter referred to as CTG, Alcor, and Belkin Components (USB 2.0 Hi-Speed PCI Card User Manual), hereafter referred to as Belkin2, Le et al. (U.S. Pub. 2003/0210532) and evidence as provided by the USB 2.0 Specification.

Regarding claim 16, Belkin teaches a computer system comprising:

A chassis defining an interior (Page 4, Figure 2 shows a PC chassis);

A first Universal Serial Bus (USB) port externally mounted to the chassis (Page 4, Figure 2 shows 4 USB ports externally mounted to the chassis via the USB hub device);

A daughter card mounted within the interior of the chassis (Page 4, Figure 2 shows the USB hub device being mounted within the interior of the chassis), and having a second USB header (interpreted as a USB connector; Page 5, #4), and a third USB header (interpreted as the inherent connective PCB traces that connects any of the external USB ports as shown in the Figure on page 1);

Belkin fails to explicitly teach a USB hub, a motherboard having a first USB header, the second USB header operative to communicate with the first USB header, a voltage regulator, and an internal USB port.

Alcor teaches a USB hub controller for providing a plurality of USB ports to connect USB devices in a cost-effective manner that provides power switch control and over-current sensing (Page 1).

Alcor also teaches a voltage regulator, the voltage regulator being operative to receive a first voltage output from the motherboard (Where the voltage regulator

receives this power on pin 10 of the hub controller chip (pages 5 – 6), and to provide in response thereto, a second, lower voltage output to the USB hub (Page 1, Section 1.2).

CTG teaches a motherboard having a first USB header (Product Features, paragraph 1; Installation Guide, Step 5-1), as well as a second header (interpreted as the connective wiring that connects the motherboard header to the external USB port as shown in the Figure on the Product Features page).

Belkin2 teaches an internal USB port (Page 5, PORT 5) for the purpose of providing USB functionality to internal USB devices.

It would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate an internal USB port as taught by Belkin2 into the USB hub device of Belkin for the purpose of adding the capability to connect internal USB devices. This would have been obvious because some internal devices (such as card readers, hard drives, etc) require an internal USB connection.

It would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to utilize the USB hub controller as taught by Alcor in controlling the USB ports of Belkin, and Belkin2 in a cost-effective manner that provides power switch control and over-current sensing. This would have been obvious in order to avoid damaging the attached USB devices.

Examiner notes that the hub controller of Alcor requires an upstream connection to a USB host controller as shown on page 3. One of ordinary skill in this art would find it obvious to make this connection by attaching the pins of the controller (via a second USB header as claimed) through the cable of CTG to the motherboard USB header of

CTG. This would have been obvious since a USB system requires a host controller to operate, and the cable of CTG would be one method of making this connection.

Le et al. teach the chassis (Figures 3A, 3B, item 100) having mounts extending into the interior thereof (Figures 3A, 3B; items 333, 334);

The daughter card has apertures formed therethrough, each of the apertures being operative to receive one of the mounts such that insertion of the mounts into ths apertures secures the daughter card to the chassis (where the PWB is interpreted in Figures 3A and 3B as item 220, and the apertures are interpreted as mounting holes (item 221).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the mounting means as taught by Le et al. into the system of Lelong et al. for the purpose of mounting the PWB in a secure manner to the chassis to prevent damage from occurring due to the PWB physically impacting the other components.

Regarding claim 17, Le et al. teach the additional limitation wherein the mounts form interference fits with the apertures when the mounts are inserted within the apertures (Figure 3A and 3B clearly show an interference fit between the mounts (items 333, 334) and the apertures (item 221)).

330 ***Response to Arguments***

Applicant's arguments with respect to claims 1 – 18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

335 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for

340 the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

345 For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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MDS

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